UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

AW

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,036	06/27/2001	Ajit V. Sathe	884.469US1	3397

21186 7590 12/31/2003

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,036	SATHE, AJIT V.	
	Examiner	Art Unit	
	Quang D Vu	2811	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 09/05/03*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17,18,21-23,26,27,31-33,36-40,42,44 and 46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17,18,21-23,26,27,31-33,36-40,42,44 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17-18 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,329,610 to Takubo et al. in view of US Patent No. 4,701,363 to Barber.

Regarding claim 17, Takubo et al. (figure 17) teach an electronic package substrate comprising:

a thin, flexible, electrically insulating film (a composite film [100] comprises flexible films [101, 102, 103]) including a conductor region (104a, 104b, 106a) to mount an integrated circuit (110);

a plurality of traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]) within the film, including within the conductor region (104a, 104b, 106a);

a plurality of lands (a portion of layer [104a] which is in contact with the bump [111]) on a surface of the film and coupled to the traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]), wherein the

lands are to mount corresponding bumps (111) of the integrated circuit (110) in a ball grid array (111); and

wherein the film (101, 102, 103) comprises a plurality of contiguous layers (layers [101] and [106a] are considered as one layer, layers [103] and [104b] are considered as another layer, and layers [102] and [104a] are considered as another layer), selected ones of which comprises a plurality of traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], a portion of layer [106a] which is not in contact with conductive pillar [107b]), and wherein the film (101, 102, 103) comprises one or more vias (105) coupled to corresponding ones of the traces.

Takubo et al. differ from the claimed invention by not showing sprocket hole in the substrate. However, Barber teaches sprocket hole, which is formed in the substrate (column 6, lines 30-38). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Barber into the device taught by Takubo et al. because it permits operations on the substrate to be properly registered by reference to the sprocket holes. The combined device shows a thin, flexible, electrically insulating film including at least one sprocket hole in the film, outside the conductor region.

Regarding claim 18, Takubo et al. teaches the film is formed of material comprising a polyimide (column 27, lines 57-59).

Regarding claim 36, Takubo et al. teach the one or more vias (105) coupled traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]) within selected layers (101, 102, 103).

3. Claims 21-23, 26-27, 37-40, 42 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,329,610 to Takubo et al. in view of US Patent No. 6,433,441 to Niwa et al.

Regarding claim 21, Takubo et al. (figure 17) teaches an electronic package comprising:

a package substrate (100) including:

a thin, flexible, electrically insulating film (a composite film [100] comprises flexible films [101, 102, 103]) including a conductor region (104a, 104b, 106a) to mount an integrated circuit (110);

a plurality of traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]), at least some of which are within the conductor region (104a, 104b, 106a);

one or more vias (105) within the film and coupled to corresponding ones of the traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]); and

a plurality of lands (a portion of layer [104a] which is in contact with the bump [111]) on a surface of the film and coupled to the traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]); and

an integrated circuit (110) including a plurality of bumps (111) coupled to the plurality of lands (a portion of layer [104a] which is in contact with the bump [111]) in a ball grid array (111).

Takubo et al. differ from the claimed invention by not showing the plurality of lands including a plurality of signal lands around the periphery of the conductor region, the plurality of lands further including a plurality of power and ground lands within a central core region of the conductor region. However, Niwa et al. (figures 1A-3B) teach a plurality of signal lands (S Land), which are formed around the conductor region, and a plurality of power (P Land) and ground (G Land) lands, which are formed within a central conductor region. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Niwa et al. into the device taught by Takubo et al. because it provides interconnection between the integrated circuit and the external device. The combined device shows the plurality of lands including a plurality of signal lands around the periphery of the conductor region, the plurality of lands further including a plurality of power and ground lands within a central core region of the conductor region.

Regarding claim 22, Takubo et al. teaches the film is formed of material comprising a polyimide (column 27, lines 57-59).

Regarding claim 23, Takubo et al. and Niwa et al. differ from the claimed invention by not showing each layer has a thickness within the range of approximately 0.15 to 0.30 millimeters. It would have been obvious to one having ordinary skill in the art at the time the invention was made for each layer has a thickness within the range of approximately 0.15 to 0.30 millimeters because it reduces the size of the device. Furthermore, it has been held that where

the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 26, the disclosures of Takubo et al. and Niwa et al. are discussed as applied to claim 21 above.

Takubo et al. further teach a plurality of lands formed directly upon a surface of the film and coupled to the traces, and the film (101, 102, 103) comprises a plurality of contiguous layers (layers [101] and [106a] are considered as one layer, layers [103] and [104b] are considered as another layer, and layers [102] and [104a] are considered as another layer), selected ones of which comprises a plurality of traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]), and wherein the film (101, 102, 103) comprises one or more vias (105) coupled to corresponding ones of the traces.

Regarding claim 27, Takubo et al. teaches the film is formed of material comprising a polyimide (column 27, lines 57-59).

Regarding claim 37, the disclosures of Takubo et al. and Niwa et al. are discussed as applied to claim 21 above.

Takubo et al. further teach the lands (a portion of layer [104a] which is in contact with the bump [111]) are to mount corresponding bumps (111) of the integrated circuit (110).

Regarding claim 38, Takubo et al. teaches the film is formed of material comprising a polyimide (column 27, lines 57-59).

Regarding claim 39, Takubo et al. teach the film (100) comprises a plurality of layers (101, 102, 103), each of the layers comprising a plurality of traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]).

Regarding claim 40, Takubo et al. teach the one or more vias (105) coupled traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]) within selected layers (101, 102, 103).

Regarding claim 42, Takubo et al. teach the film (101, 102, 103) comprises a plurality of contiguous layers (layers [101] and [106a] are considered as one layer, layers [103] and [104b] are considered as another layer, and layers [102] and [104a] are considered as another layer), selected ones of which layers comprises selected ones of the plurality of traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]), and wherein the film (101, 102, 103) comprises one or more vias (105) coupled to the traces within selected layers.

Regarding claim 44, Takubo et al. teach the one or more vias (105) coupled traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]) within selected layers (101, 102, 103).

4. Claims 31-33 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,365,421 to Debenham et al. in view of US Patent No. 6,329,610 to Takubo et al., and further in view of US Patent No. 6,433,441 to Niwa et al.

Regarding claim 31, Debenham et al. (figure 1) teach microprocessor (12), bus (18), display (24) and memory (14). Debenham et al. differ from the claimed invention by not showing a processor comprising an electronic assembly including, a thin, flexible electrically insulating film having a conductor region, a plurality of traces in the conductor region, one or more vias coupled to corresponding ones of the traces, and a plurality of lands coupled to the traces; and an integrated circuit including a plurality of pads coupled to the plurality of lands. However, Takubo et al. teach a thin, flexible, electrically insulating film (a composite film [100] comprises flexible films [101, 102, 103]) including a conductor region (104a, 104b, 106a) to mount an integrated circuit (110), a plurality of traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]) in the conductor region (104a, 104b, 106a), one or more vias (105) coupled to corresponding ones of the traces, and a plurality of lands (a portion of layer [104a] which is in contact with the bump [111]) formed directly upon a surface of the film and coupled to the traces; and an integrated circuit (110) including a plurality of bumps (111) coupled to the plurality of lands (a portion of layer [104a] which is in contact with the bump [111]) in a ball grid array (111). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Takubo et al. into the device taught by Debenham et al., since it is desirable to add functionality to the device.

Takubo et al. and Debenham et al. further differ from the claimed invention by not showing the plurality of lands including a plurality of signal lands around the periphery of the conductor region, the plurality of lands further including a plurality of power and ground lands within a central core region of the conductor region. However, Niwa et al. (figures 1A-3B) teach a plurality of signal lands (S Land), which are formed around the conductor region, and a plurality of power (P Land) and ground (G Land) lands, which are formed within a central conductor region. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Niwa et al. into the device taught by Takubo et al. and Debenham et al. because it provides interconnection between the integrated circuit and the external device. The combined device shows the plurality of lands including a plurality of signal lands around the periphery of the conductor region, the plurality of lands further including a plurality of power and ground lands within a central core region of the conductor region.

Regarding claim 32, the combined device shows the film is formed of material comprising a polyimide (Takubo et al.; column 27, lines 57-59).

Regarding claim 33, the combined device shows the film (Takubo et al; 100) comprises a plurality of layers (101, 102, 103), each of the layers comprising a plurality of traces (Takubo et al; a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]) in the conductor region (104a, 104b, 106a).

Regarding claim 46, Takubo et al. teach the one or more vias (105) coupled traces (a portion of layer [104a] which is not in contact with bump [111], a portion of layer [104b] which

is not in contact with conductive pillar [107b], and a portion of layer [106a] which is not in contact with conductive pillar [107b]) within selected layers (101, 102, 103).

Response to Arguments

Applicant's arguments with respect to claims 17-18, 21-23, 26-27, 31-33, 36-40, 42, 44 and 46 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and 703-872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
December 24, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800